REMARKS

Please consider this amendment in RCE. The amendment addresses the rejections in the final Office Action mailed by the U.S. Patent and Trademark Office on March 7, 2006. Claims 1-4, 6, 8-15 and 17-19 remain pending in the present application. Claims 1, 9 and 15 are amended. Support for the amendments can be found in the specification at least in paragraphs 0015 and 0026, and in FIG. 1. Accordingly, no new matter is added to the application. In view of the foregoing amendment and the following remarks, reconsideration and allowance of the present application and claims are respectfully requested.

Rejections Under 35 U.S.C. § 103

Claims 1-4, 6-15 and 17-19 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent Application Publication No. 2003/0035473 to Takinosawa (hereafter *Takinosawa*) in view of U.S. Patent No. 6,115,763 to Douskey *et al.* (hereafter *Douskey*). For a claim to be properly rejected under 35 U.S.C. § 103, "[t]he PTO has the burden under section 103 to establish a *prima facie* case of obviousness. It can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988) (Citations omitted). Further, "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." *In re Fritch*, 972 F.2d 1260, 1266, 23 U.S.P.Q.2d 1780 (Fed Cir. 1992).

Applicant respectfully submits that amended claims 1, 9 and 15 recite features that are not disclosed, taught or suggested by the proposed combination. Applicant respectfully submits that the proposed combination fails to disclose, teach or suggest at least "a plurality of functionally identical testers integrated with said plurality of SERDESs and said core processing logic, said testers being connected to individually test each said SERDES, each of said testers being enabled to detect performance characteristics of individual said SERDESs independently of other said testers ***and concurrently with said plurality of SERDESs, wherein a bit error rate for each said SERDES is individually identified***," and "wherein each said tester is connected to a common test bus that is integrated with said SERDESs and

said testers, ***said common test bus being separate from a data bus***, each said tester having a unique address that enables independent accessibility of said tester via said test bus, said test bus being dedicated to providing signaling for said enablement to detect performance characteristics of said individual SERDESs ***and further comprising a built in self-test (BIST) state machine integrated with said SERDESs and said testers, said BIST being connected to said test bus and being configured to sequence test operations by said individual said testers***," as recited in amended claim 1.

Applicant respectfully submits that the proposed combination fails to disclose, teach or suggest at least "a plurality of functional test interfaces (FTIs) integrally formed with said substrate, each said FTI being uniquely associated with one of said SERDESs and being connected to said parallel data inputs and outputs of said associated SERDES, said FTIs being enabled to individually and concurrently test performances of said SERDESs ***wherein a bit error rate for each said SERDES is individually identified***," and "an input/output controller (IOC) and common test bus integrally formed with said substrate, said common test bus being dedicated to providing signaling for enablement of testing, ***said common test bus being separate from a data bus***, said IOC being connected to each said FTC via said common test bus to transmit individually addressed commands to each said FTC, said IOC further being connected to exchange signals with an external device," as recited in amended claim 9.

Applicant respectfully submits that the proposed combination fails to disclose, teach or suggest at least "embedding a plurality of test interfaces within said integrated circuit such that each test interface is specific to one said SERDES with respect to exchanging parallel data, including forming each said test interface to include a test pattern generator connected to parallel data inputs of said SERDES to which said test interface is specific and further including forming each said test interface to include an error detector to receive parallel data from said SERDES to which said test interface is specific, ***wherein each of a plurality of SERDESs is individually and concurrently tested and a bit error rate of each said SERDES is individually identified***," and "embedding an input/output controller (IOC) and a test bus within said integrated circuit, including connecting said IOC between said integrated circuit output and said test bus and including linking each said test controller to said test bus, ***said test bus being separate from a data bus***," as recited in amended claim 15.

Further, Applicant respectfully submits that claims 2-4, 6 and 8, which depend either

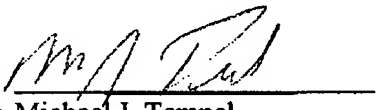
directly or indirectly from allowable claim 1; claims 10-14, which depend either directly or indirectly from allowable claim 9; and claims 17-19, which depend either directly or indirectly from allowable claim 15, are allowable for at least the reason that they depend from an allowable independent claims. *In re Fine, supra.*

CONCLUSION

Should the Examiner have any comment regarding the Applicant's response or believe that a teleconference would expedite prosecution of the pending claims, Applicant requests that the Examiner telephone Applicant's undersigned attorney.

Respectfully submitted,

Smith Frohwein Tempel Greenlee Blaha LLC
Customer No. 35856

By: 

Michael J. Tempel
Registration No. 41,344
(770) 709-0056